REMARKS

In response to the above-identified Office Action, Applicants amend the application and seek reconsideration thereof. In this response, Applicants amend Claims 1 and 2 and add new Claims 16-17. Accordingly, Claims 1-2 and 16-17 are pending.

I. Specification

The Examiner objects to the disclosure because of a typographical error requiring that "thickness a" be changed to "a thickness" on page 9, line 26 of the specification. As indicated herein, Applicants amend the specification to correct the mistake. Accordingly, Applicants respectfully request approval of the specification as amended.

The Examiner objects to the specification as being unclear since molybdenum silicide has a Fermi level of 4.25eV (N-type) (page 12, lines 10-11), yet is described as having a work function appropriate for a PMOS device (page 15, lines 22-26). As indicated herein, Applicants amend the specification to correct the mistake. Accordingly, Applicants respectfully request approval of the specification as amended.

II. Abstract

The Examiner objects to the abstract because "[it] should disclose the structure of the device instead of the method to make the device." As indicated herein, Applicants amend the abstract to correct this oversight. Accordingly, Applicants respectfully request approval of the abstract as amended.

III. Claims Rejected Under 35 U.S.C. § 112

The Examiner rejects claims 1-2 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject

matter which applicant regards as the invention. Regarding Claim 1, the Examiner contends that "a first metal gate electrode overlying a over a first gate dielectric" is unclear. Regarding Claim 2, the Examiner notes that "The integrated circuit device" has not antecedent basis. Applicants amend Claims 1-2 to address these issues. Accordingly, Applicants respectfully request approval of the claims as amended.

IV. Claims Rejected Under 35 U.S.C. § 102(b)

The Examiner rejects Claims 1-2 under 35 U.S.C. § 102(b) as being anticipated by Dash *et al*, U.S. Patent No. 4,399,605 ("Dash"). Applicants amend independent Claim 1 to overcome this rejection.

In order to anticipate a claim, the relied upon reference must disclose every limitation of the claim. Among other limitations, amended independent Claim 1 recites that the first metal gate electrode and the second metal gate electrode are separately disposed in respective ones of the first area and the second area of the semiconductor substrate.

In making the rejection, the Examiner relies on Dash to show a circuit device comprising two metal gate electrodes 56 and 50, wherein gate 56 rests on top of gate 50 as a conductive line. See Dash, Fig. 9. Thus, the cited figure fails to teach or suggest that the first metal gate electrode and the second metal gate electrode are separately disposed in respective ones of the first area and the second area of the semiconductor substrate.

Accordingly, Applicants respectfully request withdrawal of the rejection of independent Claim 1. Claim 2 depends from Claim 1. As such, Claim 2 is not anticipated at least for the same reasons as Claim 1.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attachment is captioned "Version With Markings To Show Changes Made."

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: 11/16, 2001

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CERTIFICATE OF FACSIMILE

I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office on the date shown below.

Nadya Gordon

Signature November 16, 2001 *Date*

Attachment: VERSION WITH MARKINGS TO SHOW CHANGES MADE

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

The paragraph on page 9, line 23, beginning with "After gate dielectric layer 120" has been amended as follows:

After gate dielectric layer 120 is formed, **Figure 2** shows the substrate of **Figure 1** after the further processing step of depositing metal layer 130 over the surface of substrate 100. In this embodiment, metal layer 130 is deposited to ~~thickness a~~ thickness of, for example, 500 – 2000 Å. In the embodiments that are described herein, the physical properties of at least a portion of metal layer 130 will be modified to adjust the work function for optimum NMOS and PMOS device performance. Thus, metal layer 130 will serve in its present state or in a modified state as a gate electrode. Accordingly, the thickness of metal layer 130 is scalable and should be chosen based primarily on integration issues related to device performance. Further, since in many of the embodiments that are described herein, the physical properties of metal layer 130 will be modified, care should be taken to avoid making metal layer 132 too thick so that, when desired, any modification or transformation of metal layer 130 is complete.

Four consecutive paragraphs starting at page 14, line 18, beginning with "**Figures 8-11** illustrate a second process" have been amended as follows:

Figures 8-11 illustrate a second process of forming complementary gate electrodes for optimum NMOS and PMOS device performance. In this process, as shown in **Figure 8**, semiconductor substrate or epitaxial layer 100 of a substrate has ~~P-type~~N-type well 105 and ~~N-type~~P-type well 115 formed in substrate or epitaxial layer 100 defining active area or cell region by shallow trench isolation structures 110. Overlying substrate 100 is gate dielectric 120 as described above and metal layer 130

deposited to a scalable thickness of, for example, approximately 500-2000 Å. In one embodiment, metal layer 130 is chosen to have an appropriate work function for one of an NMOS gate electrode and a PMOS gate electrode (e.g., about 4.1 electrons-volts or 5.2 electron-volts, respectively). Alternatively, metal layer 130 may require subsequent modification to tune the material to an appropriate work function for ~~an NMOS~~a PMOS device. Deposited over metal layer 130 in **Figure 8** is second metal or other material layer 160.

Figure 9 shows the structure after the further processing step of patterning second metal or other material layer 160 over a portion of metal layer 130. In this case, second metal layer 160 is patterned over the active area or cell region denoted by ~~N-type~~P-type well 115. Metal layer 130 overlying ~~P-type~~N-type well 105 is left exposed.

Next, the structure is exposed to a heat treatment, such as for example, a high temperature (e.g., 900-1000°C) or laser anneal, to drive the reaction or combination of second metal or other material layer 160 and metal layer 130 to form a metal alloy or other compound. **Figure 10** shows substrate 100 after the further processing step of subjecting metal layer 130 to a heat treatment and forming a metal alloy or other metal compound over ~~N-type~~P-type well 115. The metal alloy or metal compound 165 is selected to have an appropriate work function for ~~a PMOS~~an NMOS device. Examples of suitable metal alloys or metal compounds formed in the manner described include, but are not limited to, molybdenum silicide.

Figure 11 shows substrate 100 after the further processing step of patterning metal layers 130 and 165 into metal gate electrodes and forming ~~NMOS~~ PMOS transistor device 161 and ~~PMOS~~ NMOS transistor device 162 by a process such as described above with reference to **Figures 6** and **7**. ~~NMOS~~ PMOS transistor device 161 includes doped diffusion or junction regions 170 and ~~PMOS~~ NMOS transistor device 162

includes doped diffusion or junction regions 175. Finally, as an example, Figure 11 illustrates the coupling of ~~NMOS~~ PMOS device 161 and ~~PMOS~~ NMOS device 162 for an inverter.

IN THE ABSTRACT

The paragraph on page 23, line 2, has been replaced with the following:

A ~~method for making a~~ circuit device that includes a first transistor having a first metal gate electrode overlying a first gate dielectric on a first area of a semiconductor substrate. The first gate electrode has a work function corresponding to the work function of one of the P-type silicon and N-type silicon. The circuit device also includes a second transistor coupled to the first transistor. The second transistor has a second metal gate electrode over a second gate dielectric on a second area of the semiconductor substrate. The second gate metal gate electrode has a work function corresponding to the work function of the other one of P-type silicon and N-type silicon

IN THE CLAIMS

The claims are amended as follows:

1. (Amended) A circuit device comprising:

a first transistor including a first metal gate electrode ~~overlying a~~ over a first gate dielectric on a first area of a semiconductor substrate and having a work function corresponding to the work function of one of P-type silicon and N-type silicon; ~~and~~

a second transistor complementary to the first transistor including a second metal gate electrode over a second gate dielectric on a second different area of a semiconductor substrate and having a work function corresponding to the work function of the other one of P-type silicon and N-type silicon; and

wherein the first metal gate electrode and the second metal gate electrode are separately disposed in respective ones of the first area and the second area of the semiconductor substrate.

2. (Amended) The ~~integrated~~ circuit device of claim 1, wherein the first metal gate electrode is one of a pure metal, a doped metal, and a metal alloy.

New claims 16 and 17 have been added.